ABSTRACT OF THE DISCLOSURE

A semiconductor memory device for easily and accurately evaluating a device. The memory device has a first access mode and a second access mode. The memory device includes an entry signal generation circuit to synthesize input signals and generate a first entry signal used to enter the first access mode. A control circuit generates a first mode trigger signal in response to the first entry signal. The control circuit also receives a second entry signal used to enter the second access mode and generates a second mode trigger signal in response to the second entry signal. The entry signal generation circuit logically synthesizes the input signals in a selective manner in accordance with a selection control signal to generate the first entry signal.